Substitute for Form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*		Application Number	10/698,905
		Filing Date	October 31, 2003
		First Named Inventor:	Wolf-Dietrich Weber
		Art Unit	2825
		Examiner Name	Not yet assigned
Sheet	1 of	Attorney Docket No.	2998P035

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number — Number-Kind Code[2] (If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US 6,330,225	12-11-2001	**Weber**, Wolf-Dietrich et al.	
		US-			
		US-			
		US			
		US			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document — Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
						Y

Examiner Signature		Date Considered	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /jdr/

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/698,905
				Filing Date	October 31, 2003
				First Named Inventor:	Wolf-Dietrich Weber
				Art Unit	2825
				Examiner Name	Not yet assigned
Sheet	2	**of**	3	Attorney Docket Number	2998P035

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T^2
	2	WOLF-DIETRICH WEBER, et al., "*A quality-of-service mechanism for interconnection networks inn system-on-chips*", IEEE 2005, 6 pages.	
	3	DREW WINGARD, "*MicroNetworks-Based Integration for SOCs.*" In Design Automation Conference, 2001, pp. 673-677, 5 pages.	
	4	PAUL WIELAGE, et al., "*Networks on Silicon: Blessing or Nightmare?*" Keynote speech, Proceedings of the Euromicro Symposium on Digital System Design, Dortmund, Germany, September 2002, 5 pages.	
	5	RON HO, et al., "*The Future of Wires*". In Proceedings of the IEEE, Vol. 89, No. 4, pp. 490-504, April 2001, 15 pages.	
	6	WILLIAM J. DALLY, et al., "*Route Packets, Not Wires: On-Chip Interconnection Networks.*" In Design Automation Conference, pp. 684-689, June 2001, 6 pages.	
	7	LUCA BENINI, et al., "*Networks on Chips: A New SoC Paradigm*", In IEEE 2002, Computer, Vol. 35, No. 1, pp.70-78, 9 pages.	
	8	JIM KUROSE, "*Open Issues and Challenges in Providing Quality of Service Guarantees in High-Speed Networks*", ACM Computer Communication Review, Vol. 23, No. 1, pp.6-15, January 1993, 10 pages.	
	9	MARTIN REISSLEIN et al., "*A Framework for Guaranteeing Statistical QoS*", In IEEE/ACM Transactions on Networking, Vol. 10, No. 1, February 2002, pp.27-42, 16 pages.	
	10	HUI ZHANG, "*Service Disciplines for Guaranteed Performance Service in Packet-Switching Networks*", Proceedings of the IEEE, Vol. 83, No. 10, October 1995, pp.1374-1396, 23 pages.	
	11	DIMITRIOS STILIADIS, et al., "*Latency-Rate Servers: A General Model for Analysis of Traffic Scheduling Algorithms*", In Proceedings of IEEE INFOCOM 96, April 1996, pp.111-119, 9 pages.	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /jdr/
Based on Form PTO/SB/08B (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/698,905
				Filing Date	October 31, 2003
				First Named Inventor:	Wolf-Dietrich Weber
				Art Unit	2825
				Examiner Name	Not yet assigned
Sheet	3	of	3	Attorney Docket Number	2998P035

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	12	K. GOOSSENS, et al., *"Networks on Silicon: Combining Best-Effort and Guaranteed Services"*, In Proceeding of 2002 Design, 3 pages.	
	13	E. RIJPKEMA, et al., *"Trade Offs in the Design of a Router with Both Guaranteed and Best-Effort Services for Networks on Chip"*, In Proceedings of Design Automation and Test Conference in Europe, March 2003, 6 pages.	
	14	K. LAHIRI, et al., *"LOTTERYBUS: A New High-Performance Communication Architecture for System-on-Chip Designs"*. In Proceedings of Design Automation Conference 2003, Las Vegas, June 2001, pp.15-20, 6 pages.	
	15	WILLIAM J. DALLY, *" Virtual-channel Flow Control"*, In Proceedings of the 17th Int. Symp. on Computer Architecture, ACM SIGARCH, May 1990, Vol. 18, No. 2, pp. 60-68, 9 pages.	
	16	DREW WINGARD, et al., *"Integration Architecture for System-on-a-Chip Design"*, In Proc. of the 1998 Custom Integrated Circuits Conference, May 1998, pp 85-88, 4 pages.	
	17	AXEL JANTSCH, et al., *"Networks on Chip"*, Kluwer Academic Publishers, 2003. Cover, Title Page, Contents, (4 pp.) Chapters 1-5, (pp.3-106,) Chapters 7-8, (pp.131-172) & Chapter10, (pp. 193-213), 171 pages.	
	18	WEBER, WOLF-DIETRICH, et al., "Enabling Reuse via an IP Core-centric Communications Protocol: Open Core Protocol", In Proceedings of the IP 2000 System-on-Chip Conference March 2000, pp.1-5.	

Examiner Signature	/James Rutten/	Date Considered	03/14/2009

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /jdr/

Based on Form PTO/SB/08B (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.